An Interpolated-DFT Synchrophasor Estimation Algorithm and Its Implementation in an FPGA-based PMU Prototype

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***Abstract*—The accurate measurement of synchrophasors in static and dynamic power network conditions represents one of the main requirements of Phasor Measurement Units (PMUs). International Standards (i.e. the IEEE C37.118) are quickly evolving to drive the technological evolution of these intelligent electronic devices. In this respect, the paper presents an interpolated-DFT based synchrophasor-estimation algorithm that has been designed to meet the accuracy requirements of classes P and M defined in the recent IEEE Std C37.118-2011-1. Together with the analytical description of the main aspects of the proposed synchrophasor estimation algorithm, the paper also presents its implementation inside an FPGA-based PMU prototype. The paper finally shows and discusses some of the compliance tests of the proposed PMU prototype with respect to the above standard.**

***Index Terms* — synchrophasor measurement, phasor measurement units, discrete Fourier analysis, IEEE Std. C37.118, field programmable gate array (FPGA).**

I. INTRODUCTION

The progressive penetration of renewable energy sources (RESs) is driving major power system changes. Indeed, the promotion of RESs and, in general, distributed generation, has resulted in the need to develop new tools to manage the increasing complexity of the electrical grids and overall energy systems. The challenges associated in the near-term deployment of dedicated telecommunication infrastructures, as well as a lack of a new generation of advanced Supervisory Control and Data Acquisition (SCADA) implementing real-time control functions, are contributing to the delay of a massive integration of DG and large-scale RERs. The general consensus is that the integration of RERs into the existing electricity infrastructures requires the successful combination of real-time processes (e.g. real-time control of network power flows, energy balance via controllable energy sources, including storage and demand-side response) and new technologies (e.g. high voltage power electronic converters, grid control devices, smart meters, agent-based distributed controls), which will eventually enhance both energy efficiency and effective operation of power distribution/transmission networks.

Within this context, one of the areas receiving further attention by network operators and power systems researchers is the development/use of accurate and reliable Phasors Measurement Units (PMUs) [1,2]. Indeed, these devices compose the backbone of wide area, and local, monitoring systems to which several real-time functionalities are connected. Typical examples are: power systems stability (e.g. [3,4]), inter-area oscillations (e.g. [5]), voltage stability (e.g. [6]), relaying (e.g. [7]), real-time state estimation (e.g. [8]).

Even in the context of power distribution networks, PMUs represent fundamental monitoring tools. As discussed in [9], examples of PMU use within the context of power distribution networks operation have been presented in the literature in the following fields: protection functions, such as loss of main (e.g. [10]), fault event monitoring [11], state estimation (e.g. [12,13]), synchronous islanded operation [14,15] and power quality monitoring (e.g. [16]).

Concerning the compliance of PMUs with international standards, synchronized phasor measurements must be in agreement with the imposed by the IEEE Std. C37.118.1-2011 [17]. This standard defines synchrophasor, frequency, and rate of change of frequency (ROCOF) measurements and accuracies for the majority of operating conditions[1] under both steady-state and dynamic conditions. It is worth noting that this standard does not specify any hardware, software, or method for computing phasors, frequency or ROCOF.

Concerning the algorithms typically used in PMUs, they can be classified as DFT-based and non-DFT-based (DFT – Discrete Fourier Transform) [2]. The first category is based on the direct implementation of the DFT, or its algorithmic version – Fast Fourier Transform (FFT) –, applied to quasi-steady state signals that represent node voltages and/or branch current waveforms. DFT-based algorithms can be grouped

[1] Moreover, the IEEE Std C37.118-2011-2 [18] defines the methods and the protocols for real-time exchange of synchronized phasor measurement data.

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into one-cycle DFT estimators, and fractional-cycle DFT estimators performing recursive and non-recursive updates (e.g. [2,19]). Non-DFT algorithms for the synchrophasor estimation (e.g. based on the least-square method) have been also proposed in literature in order to improve the accuracy of phasor and frequency measurements (e.g. [20]).

Within this context, the paper presents an enhanced DFT-based synchrophasor estimation algorithm that has been designed to meet the accuracy requirements of the IEEE Std C37.118.1-2011. The proposed algorithm represents a large improvement of an interpolated DFT-based algorithm presented in [9] and inspired from [21]. The improvements refers to the correction of the harmonic interference between the DFT bins [22] as well as a computation process that has been tailored for the implementation inside a Field Programmable Gate Array (FGPA).

The structure of the paper is the following: Section II briefly provides the description of the proposed synchrophasor estimation algorithm; Section III describes the computation process specifically tailored for the implementation inside an FPGA; Section IV, by making reference to the accuracy limits of the IEEE C37.118.2011-1, provides some of the compliance tests of the obtained PMU prototype in static and dynamic conditions. Finally, Section V concludes the paper with the remarks and the conclusions.

II. The Proposed Interpolated DFT-Based Synchrophasor Estimation Algorithm

A. Requirements

The algorithm presented in this paper belongs to the category of DFT-based synchrophasor estimation algorithms. It has been conceived to satisfy the following conflicting requirements:

a. good accuracy for both transmission and distribution networks applications;
b. feasible computational complexity enabling its implementation inside an FPGA.

The last requirement had a non-negligible impact on the algorithm design. Indeed, even though algorithms performing DFT analysis in FPGA are well known, their implementation into FPGA-based synchrophasor estimators is still a challenging task even to meet the limits imposed by the 2005 edition of the IEEE Std. C37.118 [23]. Since the 2011 version of this standard has introduced more stringent accuracy requirements, there is a further need of developing enhanced DFT-based synchrophasor estimation algorithms (e.g. [24].)

Concerning the requirement (a.), as discussed in [9,15] it is worth mentioning that, compared to transmission networks, active distribution networks are much more demanding in terms of PMU performances, since they are characterized by reduced line lengths and limited power flows. With reference to the use of node voltage synchrophasors for the network state estimation, these characteristics result, in general, into very small phase differences between node voltage phasors (generally in the order of tens of mrad or less). These characteristics might be satisfied by M-class PMUs defined by the IEEE Std. C37.118.2011-1 although the required TVE limit of 1 % is still far from the operating conditions of distribution networks with reference to phase accuracy. Moreover, distribution networks are characterized by distortion levels and dynamic behaviors much more important than those of transmission networks. In addition, as active distribution networks might be operated even islanded from main transmission networks, PMUs appear a useful tool to support distribution system operators during the islanding and reconnection maneuvers (e.g. [15]). In this respect, the application of PMUs to monitor electromechanical transients, in general characterized by non-negligible deviations from the nominal frequency or sudden changes in amplitude and phase values, needs to be robust against important misestimation of synchrophasors phases and frequencies. Opposite to M-class PMUs, the P-class appears to be the most suitable to satisfy these requirements.

As a consequence, a PMU capable to be compliant with only one of the above-mentioned PMU classes does not appear to satisfy the needs associated to the use of these devices in distribution networks. In this respect, the aim of this section is to define an algorithm capable of estimating synchrophasors in most, ideally every, of the conditions for classes P and M.

B. Theoretical backgroud

The core algorithm for any PMU refers to the identification of the fundamental-frequency component contained into the sampled signal representing a general electrical quantity. As reported in [25], DFT-based tone identification algorithms are generally characterized by several levels of errors and uncertainties essentially related to: (i) the algorithm used for the tone extraction and (ii) the relevant algorithm implementation in a given hardware coupled with the time-jitter in the acquisition process.

Concerning the first point, the main source of error is the aliasing. This is usually corrected by two possible approaches: use of adequate anti-aliasing filters or increasing of the sampling frequency to values much larger than the highest spectrum component contained in the sampled signal.

Another problem arises when the sampling process is not synchronized with the fundamental component of the signal under analysis producing the so-called leakage [26]. It causes each harmonic component of the spectrum to be smeared-out over a certain range of frequencies. Since accurately synchronizing the sampling process with the fundamental frequency component of the signal is purely theoretical, several approaches have been applied in order to reduce this bias. Mainly these methods refer to the usage of (a) windowing functions that aims at mitigating the effect of long-range leakage [27] and (b) proper DFT interpolation schemes aimed to correct the effects of the short-term leakage [21,22].

Another potential cause of error is associated to the presence of harmonic interference between the DFT bins that is generally occurring when the spectrums tones are very close each other (e.g. [25,28]). Neglecting this phenomenon can cause non-negligible errors in the signal parameters estimation, particularly when high accuracy levels are required.

Basically, the proposed algorithm combines three different approaches aimed at solving the previously described sources of error and it is composed of four main steps. The first applies a suitable windowing function to the acquired signal. The second performs a DFT-analysis of the input signal. The third realize a first estimate of the signal synchrophasor by

means of an interpolated-DFT and the fourth makes an iterative correction of the harmonic interference between the DFT bins.

The peculiar characteristic of the third step is that it allows the identification of the fundamental frequency tone by using the procedure proposed in [21]. Such a procedure provides accurate results in case PMUs are operating at sampling frequencies much higher than that of the frequency tone to be identified. Indeed, this allows the elimination of aliasing effects and the use of a specific approximation finalized to deploy an interpolated-DFT. In what follows a detailed description of the synchrophasor estimation algorithm is given.

Let us consider a typical a power system signal $s(t)$ (current or voltage), characterized by a main frequency component f_1 in the range $f_0 \pm 5$Hz, being f_0 the rated frequency of the system (i.e. 50 or 60 Hz) with superposed harmonic components. The signal $s(t)$ is sampled by the PMU each $\Delta t=1/f_s$, over the time window $T=N\Delta t$ ($N \in \mathbb{N}$), sufficiently short so that the signal can be assumed stationary:

$$s(n) = \tilde{s} + \sum_{m=1}^{M} A_m \cos\left(2\pi m f_1 n\Delta t + \varphi_m\right), \quad n = 0,1,\ldots,N-1 \quad (1)$$

where $\tilde{s}$ is the DC component within the sampled time window T, A_m and φ_m are the amplitude and phase of the m-th harmonic component. As stated above, the sampling frequency f_s, is supposed to be sufficiently high to avoid aliasing effects, and disregard the presence of relevant filters that are general causing a worsening of the PMU accuracy. As in steady state the highest harmonic components that characterize the spectrum of distorted voltage/current signals in power systems rarely exceed 10 kHz, we have designed the proposed algorithm for a sampling frequency in the order of 50-100 kHz.

If $\{w(k)\}$ is the adopted window (i.e. the Hanning window in our case), then the DFT of (1), with respect to all the positive and negative spectrum images, can be expressed as:

$$S(k) = \frac{1}{B}\sum_{n=0}^{N-1} w(n)\cdot s(n)\cdot e^{-jk\beta_n},\ k = 0,1,...,N-1 \quad (2)$$

where $B = \sum_{n=0}^{N-1} w(n)$ and $\beta_n = (2\pi n/N)$.

In order to estimate the main tone frequency f_1, and the related synchrophasor, i.e. its amplitude A_1 and phase φ_1, the signal spectrum can be interpolated within a given spectrum interval that, in the case of a PMU application, surrounds f_0 (as above-mentioned $f_0 \pm 5$Hz).

In particular, as the real frequency value f_1 may fall between two subsequent DFT bins, it can be expressed as a function of the discrete DFT frequency discretization step $\Delta f=1/T$ as

$$f_1 = (k_1 + \Delta bin)\Delta f \quad (3)$$

where $-0.5 \le \Delta bin < 0.5$ is the deviation of f_1 from the relative DFT maximum k_1. In particular, as shown in [25], the Δbin can be expressed as

$$\Delta bin = \varepsilon\frac{2\alpha - 1}{1+\alpha} \quad (4)$$

where α is the ratio between the highest and second highest tone magnitudes of the DTF spectrum

$$\alpha = \frac{|S(k_1+\varepsilon)|}{|S(k_1)|} \quad (5)$$

being $\varepsilon = 1\cdot sign\left(|S(k_1+1)| - |S(k_1-1)|\right)$.

In agreement with [25], an initial estimate of the set of parameters $\{f_1, S_1, \varphi_1\}_0$ can be defined on the basis of (3) and the following relationships:

$$A_1 = 2|S(k_1)|\cdot\frac{\pi\Delta bin\cdot(1-\Delta bin^2)}{\sin(\pi\Delta bin)} \quad (6)$$

$$\varphi_1 = \angle S(k_1) - \pi\Delta bin \quad (7)$$

By now, it was implicitly assumed that the two largest spectral bins, $S(k_1)$ and $S(k_1+\varepsilon)$, were produced by the fundamental frequency only. Such an assumption is not generally true since the contribution of other harmonics of $s(t)$ could influence these two bins [22]. Additionally, the values of $S(k_1)$ and $S(k_1+\varepsilon)$ might be influenced by the tails produced by other negative spectrum images. This phenomenon, also known as self-interaction [28], is related to the fact that, when a spectrum has a main component at a small frequency compared to the sample rate (i.e. close to zero, as in our case), the positive and negative frequency images of the main spectrum component may overlap in the frequency space. In this way, the peaks of the positive frequency image, and consequently the Δbin estimate, could be biased by its negative equivalent.

In general, the DFT spectrum might be expressed in terms of the contribution of each harmonic component in the positive and negative spectrum range. Since in our case a meaningful hypothesis is that the self-interaction is the most relevant phenomenon, we could disregard other harmonics contribution. With this hypothesis, the following relation can be derived:

$$S(k) \approx \frac{1}{B}\left[V_1\cdot W\left(\frac{k_1\Delta f - f_1}{\Delta f}\right) + V_1^*\cdot W\left(\frac{k_1\Delta f + f_1}{\Delta f}\right)\right] \quad (8)$$

where $V_1 = (A_1/2j)e^{j\varphi_1}$, V_1^* is its complex conjugate and $W(f)$ represents the Fourier transform of the selected windowing sequence.

Using equations (3) and (8), the highest and second highest bins can then be expressed as:

$$S(k_1) \approx \frac{1}{B}\left[V_1\cdot W(-\Delta bin) + V_1^*\cdot W(2k_1 + \Delta bin)\right] \quad (9)$$

$$S(k_1+\varepsilon) \approx \frac{1}{B}\left[V_1\cdot W(\varepsilon - \Delta bin) + V_1^*\cdot W(2k_1 + \varepsilon + \Delta bin)\right] \quad (10)$$

where the harmonic interference coming from the corresponding negative spectrum image is represented by:

$$A = V_1^*\cdot W(2k_1 + \Delta bin) \quad (11)$$

$$B = V_1^*\cdot W(2k_1 + \varepsilon + \Delta bin) \quad (12).$$

Using the initial parameter sets $\{f_1, S_1, \varphi_1\}_0$ given by (3), (6) and (7), the amount of self-interaction between the negative and positive spectrum images can be computed and subtracted form the original bins to obtain an improved α estimate:

$$\alpha' = \frac{\left|S(k_1+\varepsilon)-A\right|}{\left|S(k_1)-B\right|} \quad (13).$$

This process can be iterated a predefined number of times or until a given convergence criterion is achieved. Once the iterative process is terminated, a final and more accurate estimation for the set of parameters $\{f_0, S_1, \varphi_1\}$ can be given.

III. Implementation in a FPGA-based Hardware Platform

The algorithm has been implemented into a National Instruments Compact-Rio embedded control and acquisition system equipped with (i) a real-time microcontroller, characterized by a 800 MHz real-time processor with 4 GB nonvolatile storage and 2 Ethernet network interfaces, and (ii) a reconfigurable FPGA (Field Programmable Gate Array) chassis equipped with a Virtex-5 LX110 FPGA. The FPGA has the following characteristics: clock frequency of 200 MHz, 17'280 slices (each one of them containing 4 LUTs and 4 flip-flops), 4'608 kbits of RAM and 64 DSP48E slices (each one characterized by a 25 x 18 multiplier, an adder and an accumulator). The communication between the RT microcontroller and the FPGA is guaranteed by a 512 MB DRAM memory shared by the two hardware resources.

The sampling of the voltage and current waveforms has been realized by means of 2 parallel 24-bits Delta-Sigma converters, characterized by a sampling rate up to 50 kS/s and an input signal dynamic of 300 V_{RMS} for the voltage and 5 A_{RMS} for the current. These input modules are directly controlled by the FPGA chassis and operated together with the availability of the UTC-GPS Pulse Per Second signal provided by a stationary GPS unit with a time uncertainty of ±100 ns.

A representative hardware configuration of the proposed PMU is illustrated in Figure 4.

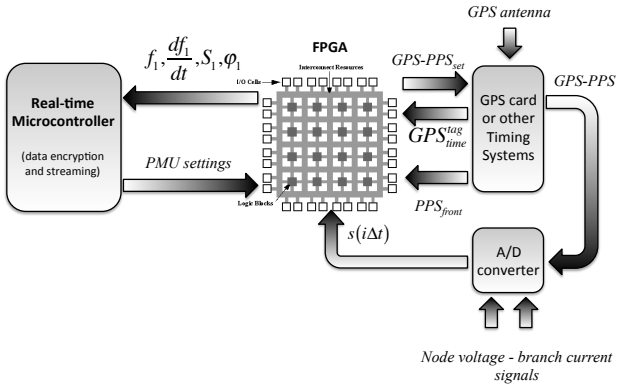

Fig. 1. Implementation of the synchrophasor estimation algorithm into the NI CompactRio embedded system.

The synchrophasor estimation algorithm has been fully developed on the FPGA and its implementation has been split in 3 parallel process performing (i) the GPS synchronization and generation of a sub-PPS square waveform synchronized with the UTC-PPS signal, (ii) the pipelined signal acquisition for a duration corresponding to the observation window T and (iii) the synchrophasor estimation based on the previously described algorithm up to the maximum rates imposed by [17].

As it can also be seen from Figure 1, the microcontroller is almost passive since the whole synchrophasor estimation process is performed by the FPGA. Consequently the microcontroller can be dedicated to other PMU functionalities like data encryption and local protection/control functionalities.

As the sampling clock is free running with respect to the GPS time reference, a further step is applied on the FPGA level in order to improve the estimation of the synchrophasor phase φ_1. Indeed, the synchrophasor phase is known with an accuracy that, neglecting the uncertainties due to the DFT, is correlated to the sampling time step Δt. In particular, such an uncertainty corresponds, for an f_s=50 kHz and a rated system frequency of 50 Hz, to 2π mrad (0.36 deg), a value that is too large. Therefore, the algorithm applies the following procedure. Since the sampling of $s(t)$ is triggered in correspondence of a rising edge of a PPS synchronized square waveform, it is possible to freeze the UTC time stamp of the first sample of $s(t)$ and calculate the time delay between the rising edge of the trigger signal and the first sample of the window. Such estimation provides a further and substantial correction of the phase φ_1.

IV. Compliance Verification with the Limits of the IEEE Std. C37.118.2011-1

The experimental validation of the developed PMU has been carried out by using reference waveforms generated by means of a GPS-synchronized function generator based on the PXI (PCI eXtensions for Instrumentation) architecture. In particular, the system is composed by a National Instruments PXI 1042Q chassis on which the following devices are connected: (i) NI PXI-5441 arbitrary waveform generator, (ii) NI PXI-6682 GPS IRIG-B timing and synchronization module, (iii) NI PXI-6281 high accuracy data acquisition board and (iv) NI PXI-8110 high-performance Intel Core 2 Quad Q9100-based embedded controller.

Since the PXI architecture of the system, that allows sharing 10 MHz TTL clocks, it has been possible to accurately synchronize the generation of the output signals with the GPS reference with an accuracy of less than 25 ppm and a skew less than 1 ns. Therefore, the time accuracy of the signals generated by this system can be assumed as a reference. Concerning the estimation of the reference signals amplitude, as the generation card does not meet the necessary accuracy levels, it has decided to re-sample the generated reference signals by means of a accurate data acquisition card which sampling has been also synchronized with the GPS reference.

This architecture allows, therefore, generating both steady state and transient reference signals containing single and multi tone waveforms. Most of the tests described in [17] for both static and dynamic conditions have been specifically implemented in the above hardware and a brief description of obtained results is given below with reference to the PMU prototype.

A. Static tests

Relatively to steady state conditions, two cases have been analyzed as illustrated in [17]: (i) single-tone signals characterized by a frequency ranging between 45 Hz to 55 Hz and (ii) distorted signals characterized by a single superposed harmonic component. Concerning this last case, the standard [17] imposes for class-M PMUs a reference signal characterized by a 10% single harmonic superposed to the nominal frequency tone.

The TVE and frequency error (FE) were analyzed over a 1 minute window of synchrophasor estimations. They are reported as a function of the nominal frequency and the harmonic component frequency for single tone and distorted signals respectively. As it can be observed, the obtained TVE and FE are almost two orders of magnitude below the required limits.

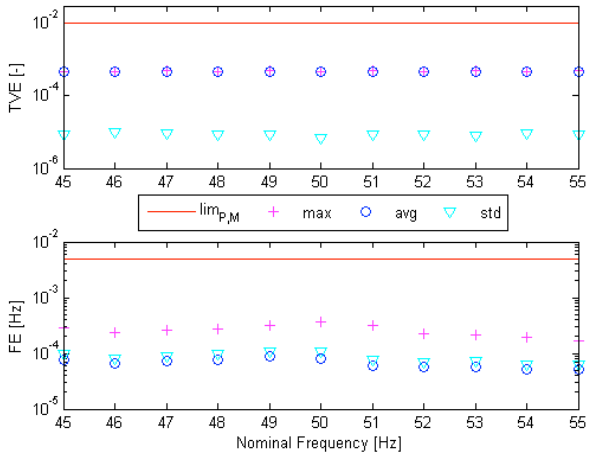

Fig. 2. PMU TVE and FE with reference to static tests with single tone signals.

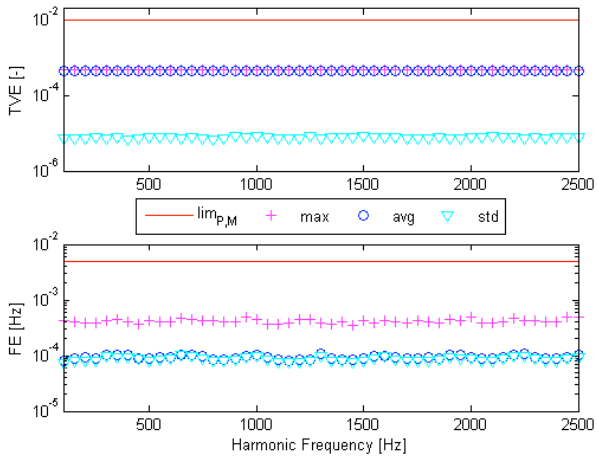

Fig. 3. PMU TVE and FE with reference to static tests with distorted signals.

B. Dynamic tests

In this section the assessment of the PMU compliance with some of the tests imposed by [17] concerning dynamic conditions, is illustrated. In particular, the reference signal generator has been programmed to generate single-tone signals characterized by (i) frequency-sweep and (ii) phase and amplitude modulations. Relatively to (i), the frequency has been linearly varied in the range between 45 and 55 Hz at a rate of ±1 Hz/s. On the other hand, as for (ii), several modulating frequencies in the range between 0.1 and 5 Hz have been tested.

Concerning the frequency sweep test, the TVE and FE still exhibit values almost two orders of magnitude below the limit. Concerning the FE, during the frequency time-derivative change, it exceeds the imposed limit during for a time of 23 ms that is below the imposed limit of 40 ms for a synchrophasor reporting rate of 50 estimations-per-second.

Concerning the modulation tests, the TVE is always well below the limits as well as the FE (concerning this last quantity, it is worth reminding that, for class P, the test has to me extended up to 3 Hz modulating frequencies with a limit error of 0.06 Hz whilst, for class M, it has to me extended up to 5 Hz modulating frequencies with a limit error of 0.3 Hz).

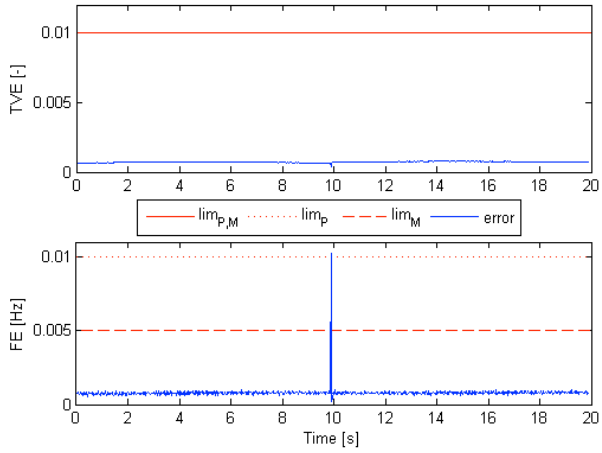

Fig. 4. PMU TVE and FE with reference to the frequency sweep dynamic test.

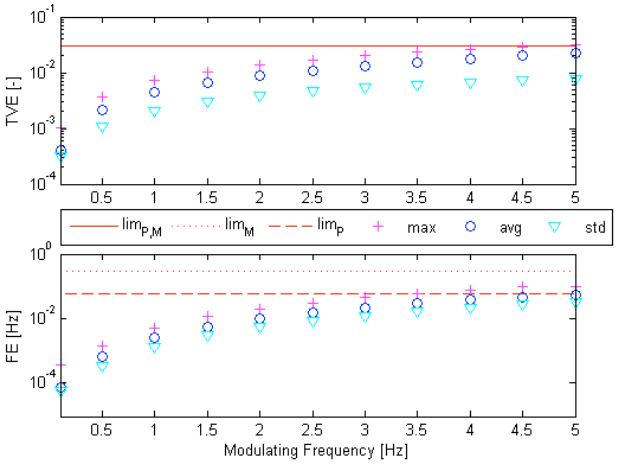

Fig. 5. PMU TVE and FE with reference to amplitude and phase modulations.

V. Conclusions

The paper has presented an interpolated-DFT-based synchrophasor estimation algorithm integrating, also, a

process for the harmonic interference correction. The algorithm has been designed for its full implementation into an FPGA.

The developed PMU prototype has been described together with its experimental characterization with reference to the static and some of the dynamic tests imposed by the IEEE C37.118.2011-1. The obtained results have shown that the obtained PMU is compliant with limits imposed by the above-mentioned standards concerning both P and M classes.

Therefore, the developed PMU exhibits peculiar characteristics enabling its use in several applications ranging from accurate monitoring and protection of transmission and distribution networks.

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